PHP/PHD3055E

TrenchMOS™ standard level FET

Rev. 06 — 25 March 2002 **Product data**

1. Description

N-channel standard level field-effect power transistor in a plastic package using TrenchMOS™[1] technology.

Product availability:

PHP3055E in SOT78 (TO-220AB)

PHD3055E in SOT428 (D-PAK).

2. Features

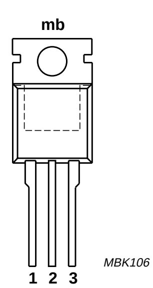
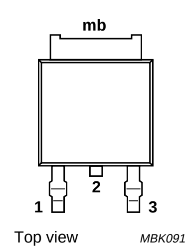
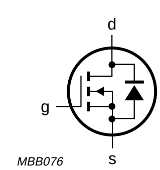
- Fast switching
- Low on-state resistance.

3. Applications

- DC to DC converters
- Switch mode power supplies.

4. Pinning information

Table 1: Pinning - SOT78, SOT428 simplified outline and symbol

Pin	Description	Simplified outline		Symbol
1	gate (g)			
2	drain (d) [1]			
3	source (s)			
mb	mounting base, connected to drain (d)	SOT78 (TO-220AB)	SOT428 (D-PAK)	

[1] It is not possible to make connection to pin 2 of the SOT428 package.

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

5. Quick reference data

Table 2: Quick reference data

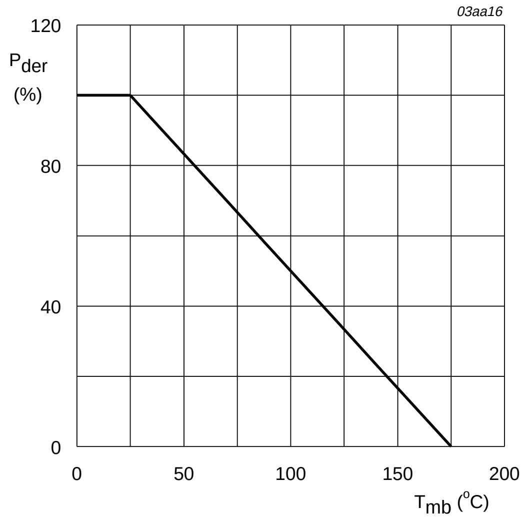
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	60	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	-	10.3	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	33	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 5.5 A	120	150	mΩ

6. Limiting values

Table 3: Limiting values

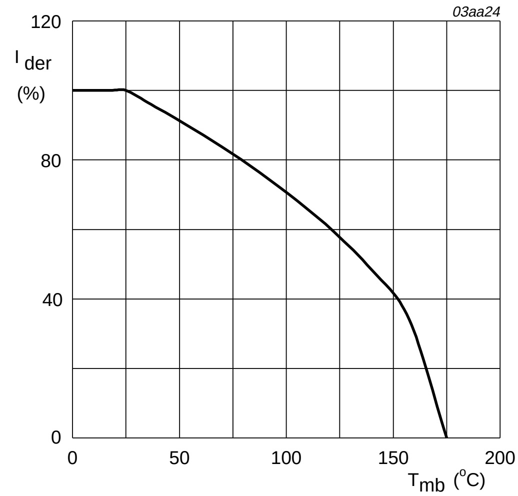
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	60	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	60	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	10.3	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	-	7.3	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	41	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	33	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	10.3	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	41	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 3.3 A; t_{AL} = 0.22 ms; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C	-	25	mJ
$I_{DS(AL)S}$	non-repetitive avalanche current	unclamped inductive load; V_{DD} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; Figure 4	-	10.3	A



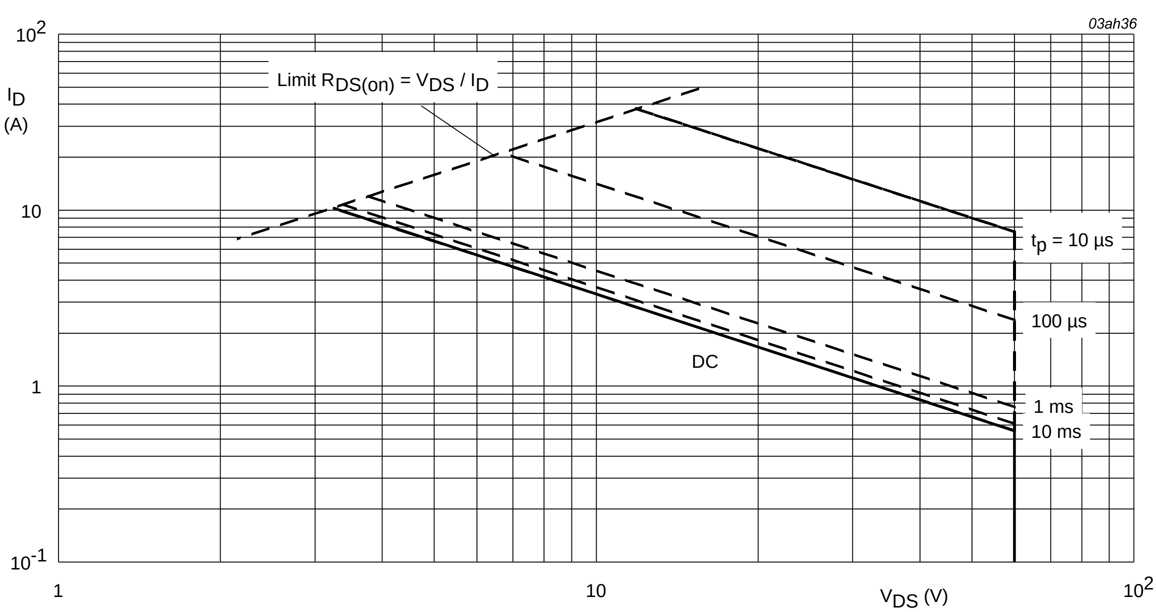
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



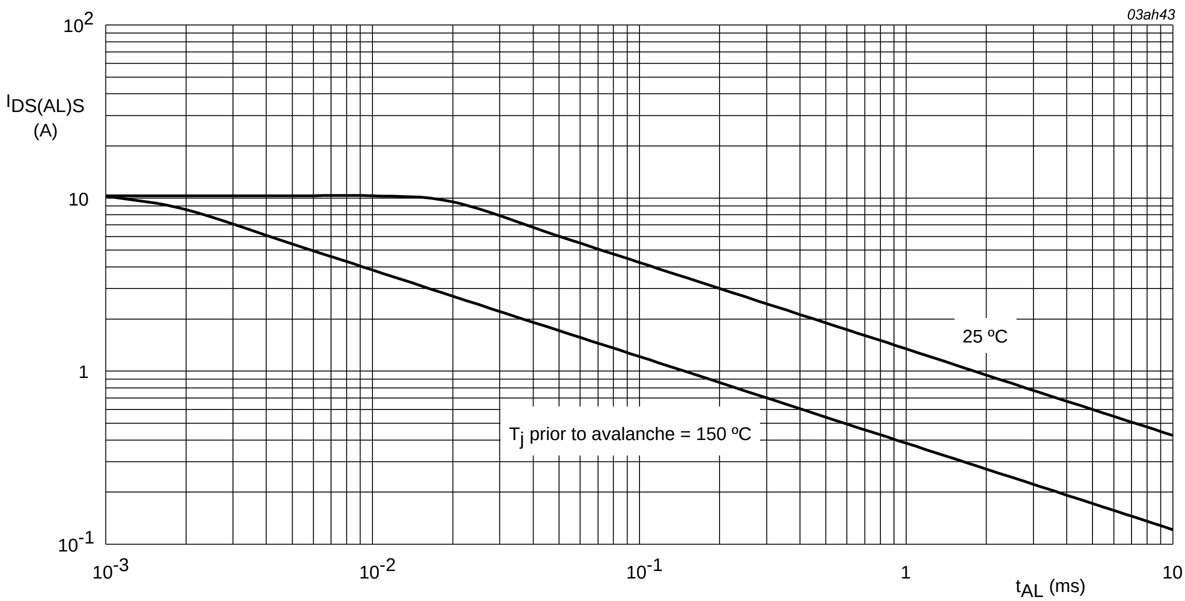
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; $V_{DD} \leq 25$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V; starting $T_j = 25$ °C and 150 °C.

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 5	-	-	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT78 package; vertical in still air	-	60	-	K/W
		SOT428 package; SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
		SOT428 packages; SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

7.1 Transient thermal impedance

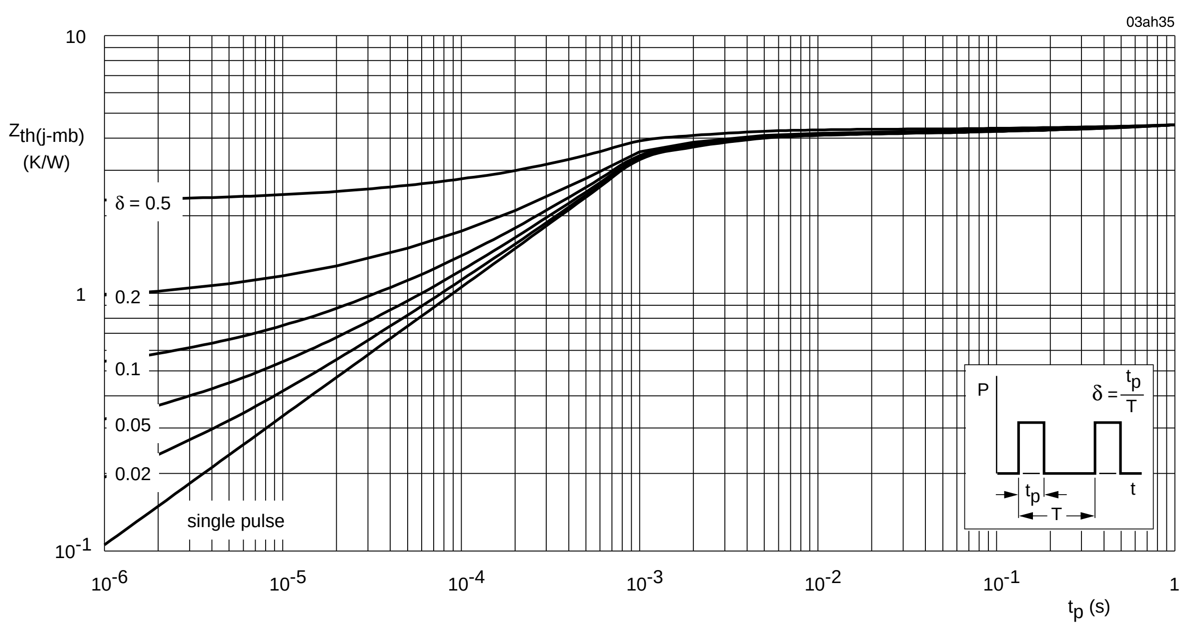


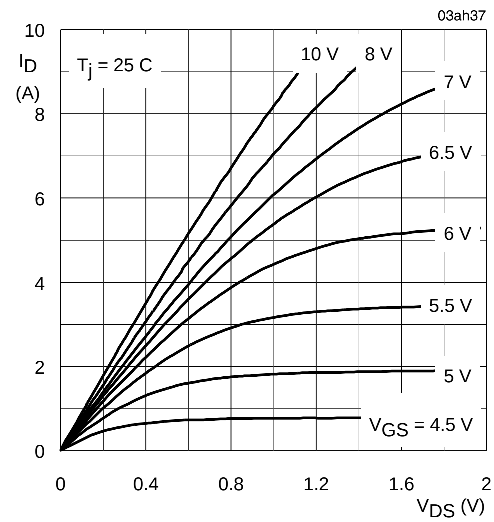
Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

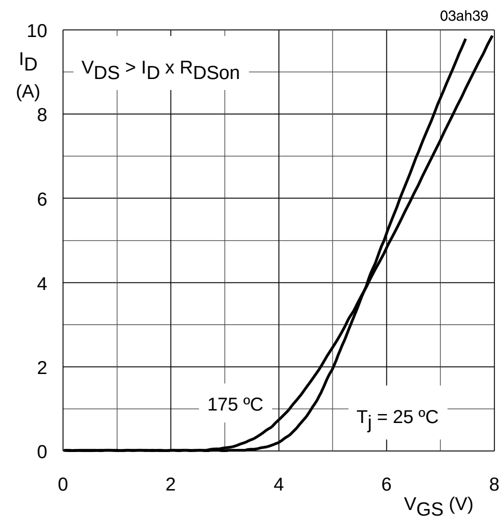
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	60	-	-	V
		T_j = –55 °C	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 10				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	6	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A; Figure 8 and 9				
		T_j = 25 °C	-	120	150	mΩ
		T_j = 175 °C	-	250	315	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 10 A; V_{DD} = 44 V; V_{GS} = 10 V; Figure 14	-	5.8	-	nC
Q_{gs}	gate-source charge		-	1.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	190	250	pF
C_{oss}	output capacitance		-	55	80	pF
C_{rss}	reverse transfer capacitance		-	40	50	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 2.7 Ω; V_{GS} = 10 V; R_G = 5.6 Ω; resistive load	-	3	10	ns
t_r	rise time		-	26	35	ns
$t_{d(off)}$	turn-off delay time		-	8	15	ns
t_f	fall time		-	10	20	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 13	-	1.1	1.5	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	32	-	ns
Q_r	recovered charge		-	50	-	nC



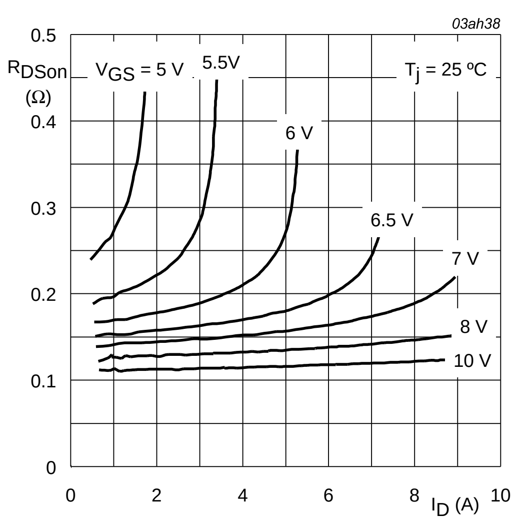
T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



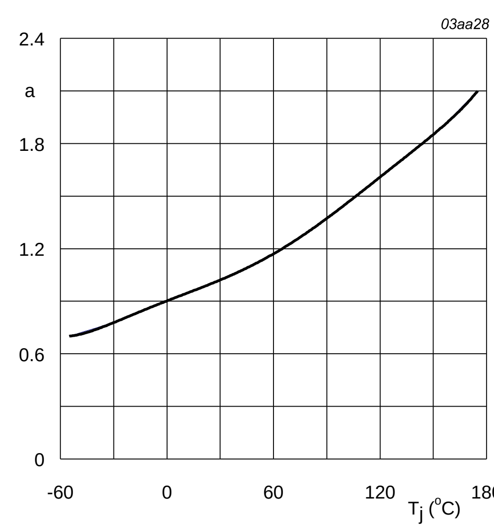
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



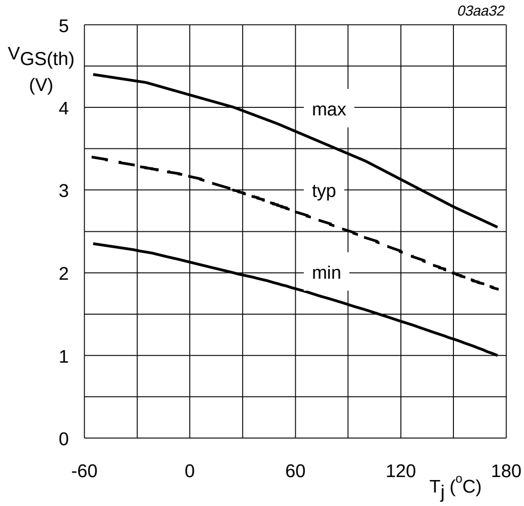
T_j = 25 °C

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



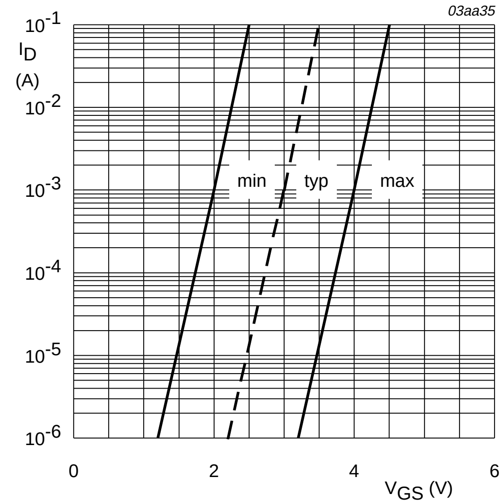
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



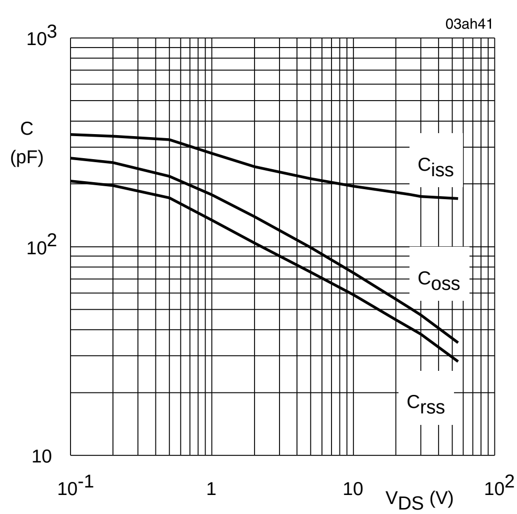
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



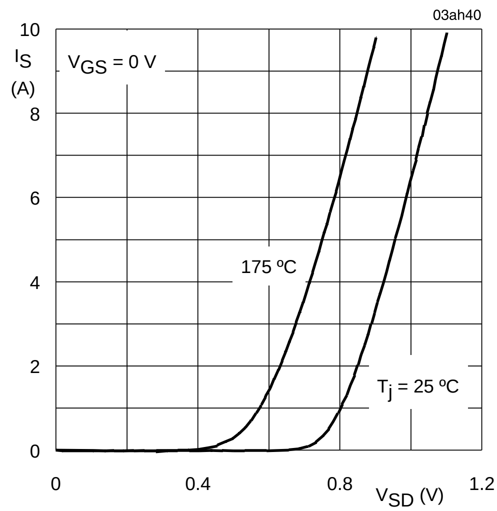
T_j = 25 °C; V_{DS} = 5 V

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



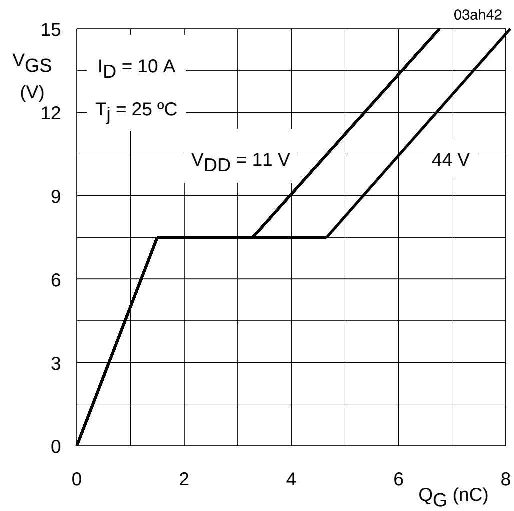
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

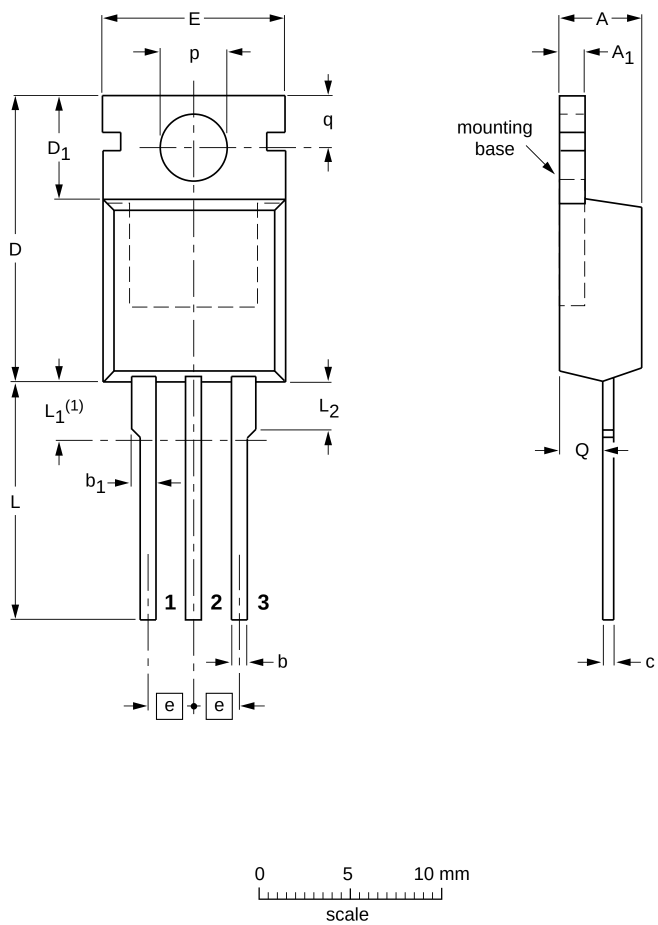


I_D = 10 A; V_{DD} = 11 V and 44 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	$L_1^{(1)}$	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

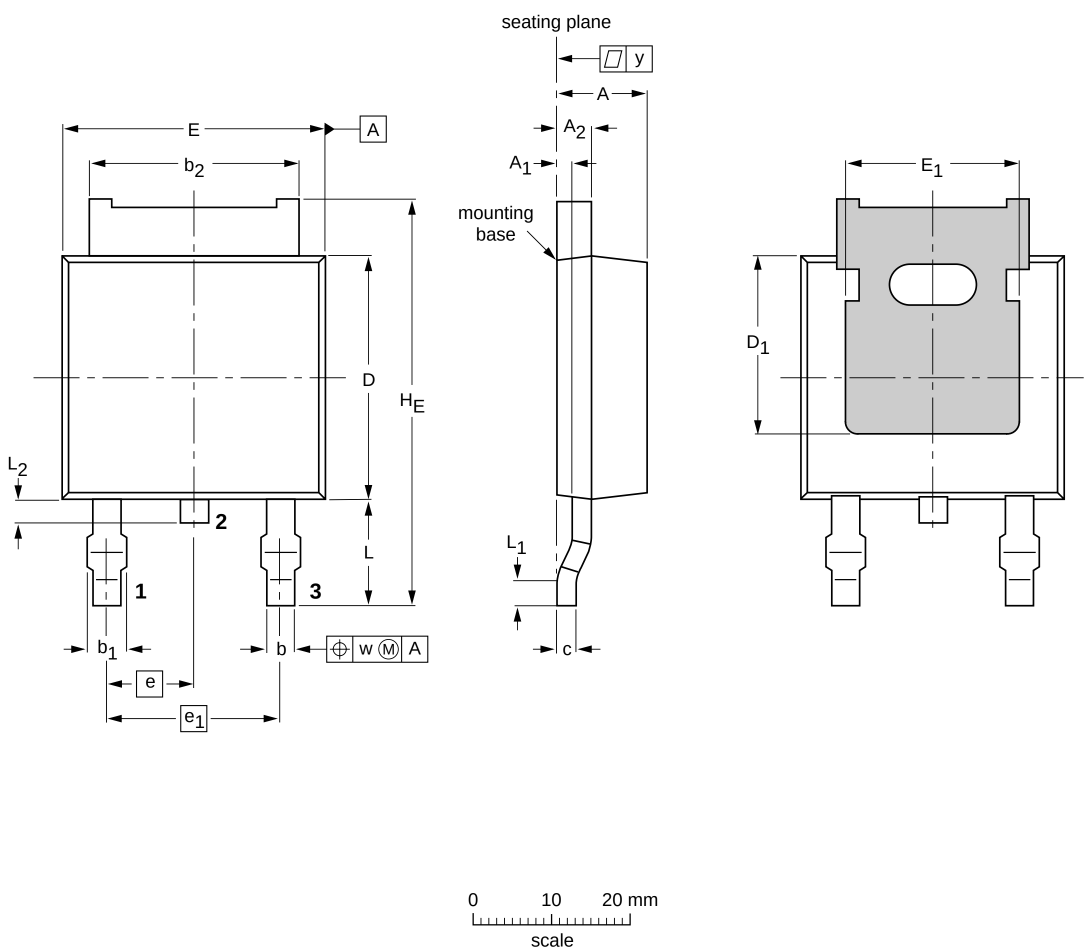
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~00-09-07~~ 01-02-16

Fig 15. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 (1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
06	20020325	-	**Product data; sixth version; supersedes PHD_PHP3055E_5 of 1 August 1999.** **Modifications:** • The format of this specification has been redesigned to comply with Philips Semiconductors’ new presentation and information standard

11. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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